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B. E. (Seventh Semester) Examination, Nov.-Dec. 2021

(New Scheme)

(Et&T Engg. Branch)

DIGITAL CIRCUIT DESIGN with VERILOG HDL

Time Allowed : Three hours

Maximum Marks : 80

Minimum Pass Marks : 28

Note : *Part (a) of each question is compulsory. Attempt any* ***two*** *parts from (b), (c) and (d) of each question.*

Unit-I

1. (a) Define and declare a module in Verilog. 2

(b) Write notes on System Task and Compiler Directives. 7

(c) Explain the lexical conventions of Verilog. 7

(d) Differentiate between Verilog and VHDL. Explain the design flow of any digital IC. 7

Unit-II

2. (a) State two procedural constructs of behavioural modelling in Verilog. 2

(b) What is the difference between blocking and non blocking assignment? Show it with example. 7

(c) Explain the different types of modelling in Verilog. 7

(d) Write short note on different operators and operands used in Verilog. 7

Unit-III

3. (a) Differentiate between Tasks & functions. 2

(b) What are Nets data types that can be used to model physical connection in Verilog? 7

(c) Write the Verilog code for 2 : 4 decoder and 4 : 2 encoder in behaviour modelling. 7

(d) Write Verilog code for BCD to 7 segment display code converter using CASE statement. 7

Unit-IV

4. (a) Write the code for D flip flop. 2

(b) Write a verilog code for BCD counter. 7

(c) Model a 4 bit linear feedback shift register using Verilog HDL. 7

(d) Write Verilog code for JK flip flop. 7

Unit-V

5. (a) What is one hot encoding? 2

(b) What are two types of state machine for designing FSM? Differentiate between them. 7

(c) Write all design steps necessary to design a state machine. Show it with an example. 7

(d) Explain Dice game with block diagram. 7